User's guide of four-bit code POST card

This User's guide is fit for the common computer post card(SLDC006, SLDC007, SLDC010, SLDC011)

（There are editions in Chinese for you to choose）

● Not only diagnose the trouble of main board but also the trouble of the POST card, keep users from misunderstanding .

● More compatible with main board PIV, end the history that the POST card is unable to work as the main board update constantly.

● You can consult the code that has run; Press the switch once and the code pauses

● It do no harms to device while insert the card wrongly with a speaker on the card to remind you there is an error, SMD device that protect your hands.

● Test the speed of PCI and ISA bus of the computer, you will get the result as soon as you test it. It can help you not suffer losses when you buy the computer, and also help you sell the computer that has a fast bus speed at good price. .

I、Front view

II、Implication of word/number of four-bit code post card

word/NUM	Description

0 － － －	Start automatic diagnosis after it displayed for about half a second
1－－－	The first function symbol of main menu ,then enter code consulting function after it displayed for about half a second
2－－－	The second function symbol of main menu , then display the reference speed of bus after it displayed for about half a second
3－－－	The third function symbol of main menu ,display the versionnumber"5002" after it displayed for about half a second
4－－－	The fourth function symbol of main menu, start to test the card and display from "0000"、"1111" to "FFFF" after it displayed for about half a second
5－－－	The 5th function prompt ,start self-test after the prompt displayed for about half second. .As long as each of 4 bits can display symbols, no matter what it displays, the POST process passed. Because of the POST content has been enhanced a lot, plenty of symbols are especial . you can pay no attention to it.
－P C I	It indicates that the slot you insert the card is PCI slot, and wait for you to consult the next code by pressing function switch.
－I S A	It indicates that the slot that you insert the card is ISA slot. And wait for you to consult the next code by pressing function switch.
－－－P	Waiting for you to consult the next code by pressing the function switch. After it displayed for half a second, the code will be displayed, and the first two bits indicates the hexadecimal error code .The last two bits indicates the ordinal number of the code.
P－－－	Waiting for you to consult the preceding code by pressing the function switch. After it displayed for half a second, the code will be displayed, and the first two bits indicates the hexadecimal error code, the last two bits indicates the ordinal number of the code.
－E n d	The last code(ordinal number limit: 0-47) forward consulting is displayed; press and hold the function switch for some 0.8 second, then enter the backward consulting mode and display "P- - -", after half a second, the code is displayed, the first two-bit code indicates the 47th POST code, the last two-bit code(47) indicates the ordinal number of the code; if press and hold the function switch for about 0.8 second twice, it will exit the code consulting and enter the second function of main menu, at the same time displayed "2- - -", then display the reference speed of PCI/ISA bus in decimal in half a second.
E n d－	The first code (ordinal number limit : 0-47) backward consulting is displayed; Press and hold the function switch for 0.8 second, then enter the forward consulting mode and display"- - -P", after half a second, the code is displayed, the first two-bit code indicates the zero code; the last two-bit code (00) indicates the ordinal number of the code. If press and hold the function switch for about 0.8 second twice, it will exit the code consulting and enter the second function of main menu, at the same time displayed"2- - - ", then display the reference speed of PCI/ISA bus in decimal in half a second.

III、Flow Chart

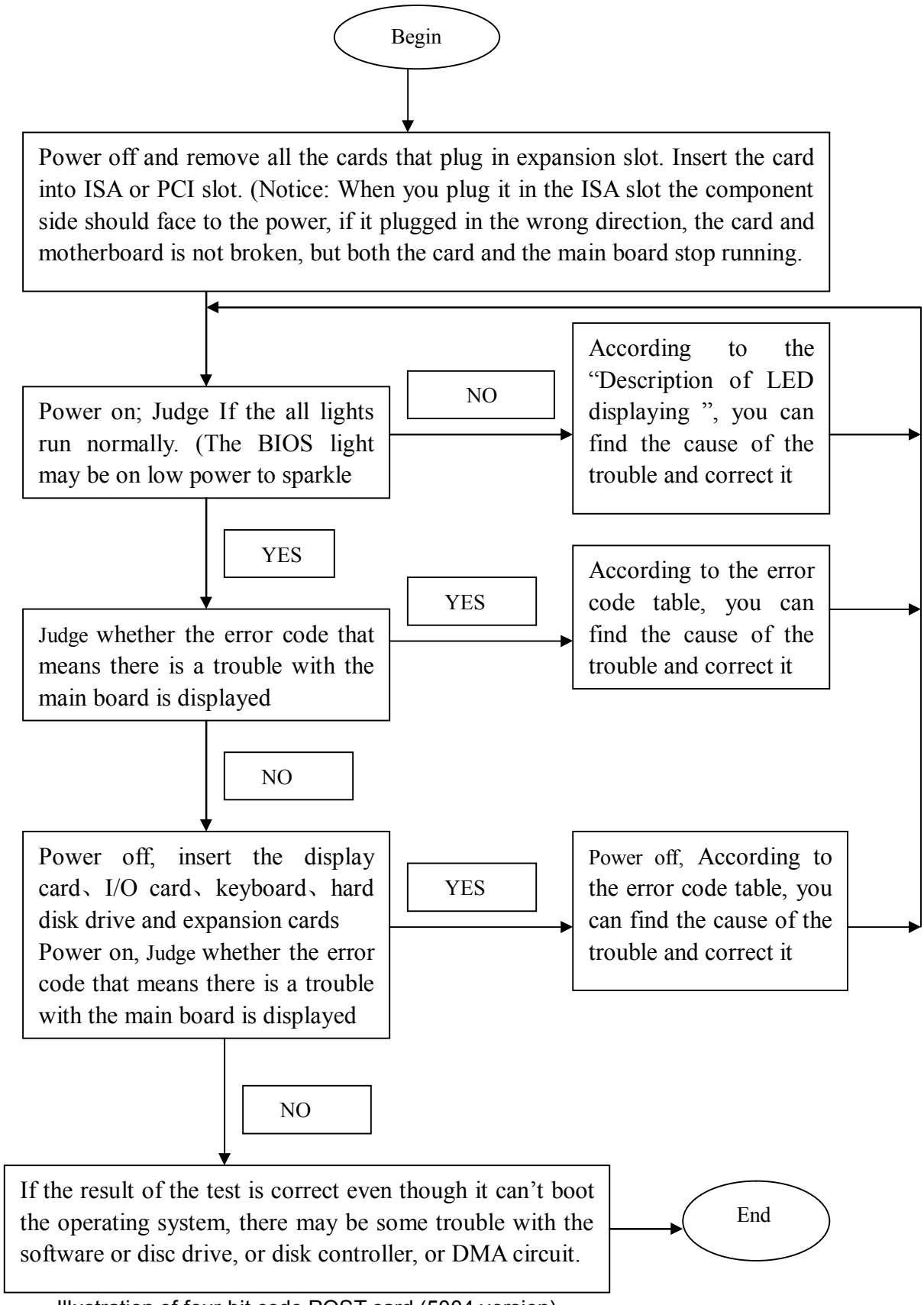
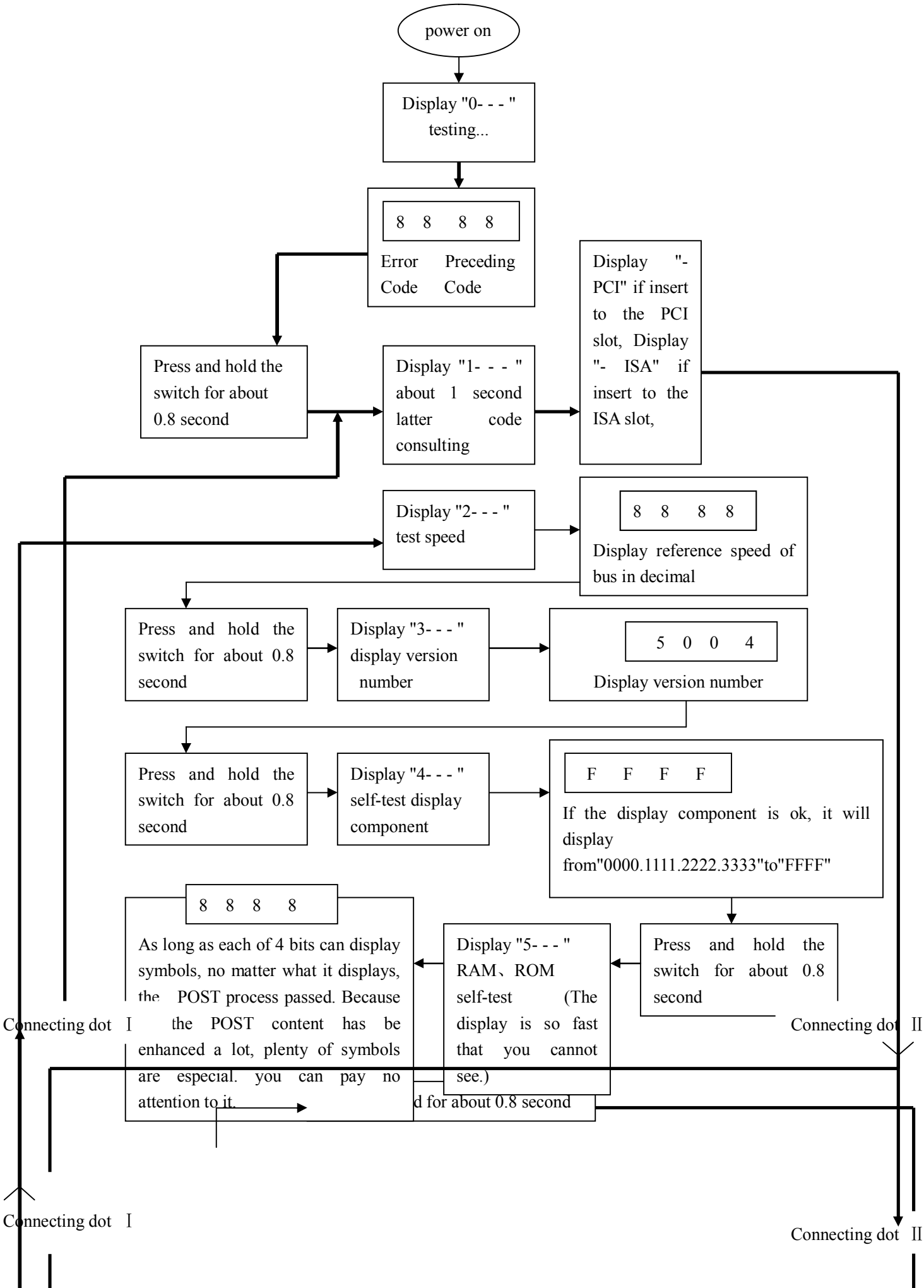
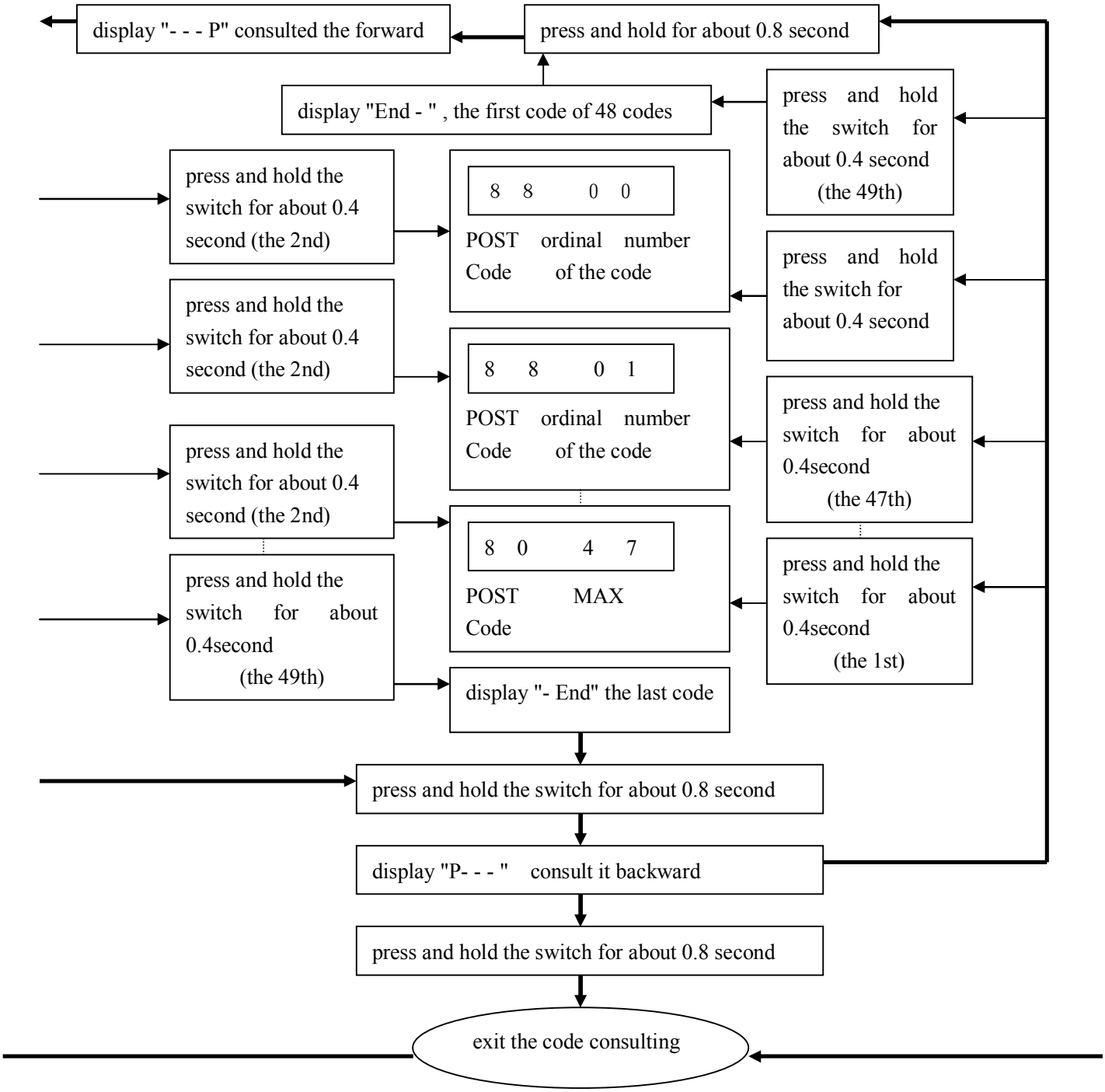


Illustration of four-bit code POST card (5004 version)


power on
Display "0- - - " testing...
8 8 8 8
Error Code
Preceding Code
Press and hold the switch for about 0.8 second
Display "1- - - " about 1 second latter code consulting
Display "- PCI" if insert to the PCI slot, Display "- ISA" if insert to the ISA slot,
Display "2- - - " test speed
8 8 8 8
Display reference speed of bus in decimal
Press and hold the switch for about 0.8 second
Display "3- - - " display version number
5 0 0 4
Display version number
Press and hold the switch for about 0.8 second
Display "4- - - " self-test display component
F F F F
If the display component is ok, it will display from"0000.1111.2222.3333"to"FFFF"
8 8 8 8
As long as each of 4 bits can display symbols, no matter what it displays, the POST process passed. Because the POST content has be enhanced a lot, plenty of symbols are especial. you can pay no attention to it.
Display "5- - - " RAM、ROM self-test (The display is so fast that you cannot see.)
Press and hold the switch for about 0.8 second
Connecting dot I
Connecting dot II
Connecting dot I
Connecting dot II



code analysis clew

The codes that can be consulted are last 0 to 47 codes that take relative longer time in the POST process, not all the code need to be consulted.(some main board output millions of codes or the same code appears many times), If the same code take different time to run in different running courses on the same main board , the POST card not always use it as code that can be consulted. The main board is of the good stability If the 47 codes that consulted in different running courses on the same main board are the same, and the last 47th code has passed the POST, but this situation is rare.

IV、Obligatory content

The error code table is in the order of the code value that from small to big. The sequence that the code displays is decided by BIOS of the motherboard;

2. Four-bit code can be divided to two two-bit codes .The one is made of the thousands digit and the hundreds digit ;The other is made of the tens digit and units digit .According to the two two-bit codes, Not only you can know the posting for computer can not pass the units that the thousands digit and the hundreds digit point out, but also you can know that the post for computer can pass the units at last that the tens digit and the units digit point out;
3. Code haven't be defined is not included in the table;
4. For the different BIOS (such as AMI、Award、Phoenix), a Code has different meanings. So make sure that which kind of BIOS you are testing. Or view the user's guide, or See it on the BIOS IC on the motherboard;
5. There is only some code displayed when you insert the card into the PCI slot on a few motherboards, but when it plugged into the ISA slot, all the code could be displayed. At present, it has be discovered that the code is displayed when you insert the card into the PCI slot of several computers which has registered trade mark, but not ISA. So You'd better try it on the other slot if the code is not displayed. In addition, on the different PCI slots of a board, some could display the code, for example, the code is displayed and goes from "00" to "FF" when you insert the card into the PCI slot, which is near to the CPU on motherboard DELL810, but if in the other slot , the code would stopped at the port "38";
6. The time that reset message output needed is not always in-phase, so sometimes the code is displayed when the card in the ISA, but it is stopped at the origination code when in the PCI.;
7. As there are more and more kinds motherboard, and the code of BIOS POST is updated ceaselessly, so the meanings of error codes is just for reference;

V、Description of LED displays

LED	Type	Description
CLK	Bus clock	Lights when the power is applied to the empty board (even without CPU) , or else there is no message.
BIOS	Base input/output read	LED that turn on and off when the board is powered on, as CPU is reading to BIOS.
IRDY	Manager is ready	LED that turn on and off when there is a message.
OSC	Oscillation	Lights when the board is powered on, or else the crystal oscillation circuit is broken, and has no OSC

		message.
FRAME	Frame periods	Lights all the time. Turn on and off only when there is a circular frame message.
RST	Reset	Lights only for half-second when you slide the power switch or the reset switch. If it is lit all the time, check the following: make sure that the reset pin is plugged properly, or the reset circuit is broken.
12V	Power	Lights once the board is powered on, if it is not lit, that means the short circuit occurs on motherboard, or voltage can't up to 12V.
-12V	Power	The same as"12V"
5V	Power	The same as "12V"
-5V	Power	The same as "12V" (-5V is output only in ISA slot.

VI、Error code table

CODE	Award	AMI	Phoenix4.0/Tandy3000
00		Code copying to specific areas is done. Passing control to INT 19h boot loader next.	
01	Processor Test 1, Processor status (1FLAGS) verification. Test the following processor status flags: carry, zero, sign, overflow. The BIOS sets each flag, verifies they are set, then turns each flag off and verifies it is off.		CPU is testing the register inside or failed, please change the CPU and check it.
02	Test All CPU Registers Except SS, SP, and BP with Data FF and 00		Verify Real Mode
03	Disable NMI, PIE, AIE, UEI, SQWV. Disable video, parity checking, DMA.	The NMI is disabled. Next, checking for a soft reset or a power on condition	Disable Not masked Interrupt (NMI)

	Reset math coprocessor.		
	Clear all page registers, CMOS shutdown byte.		
	Initialize timer 0, 1, and2, including set EISA timer to a known state.		
	Initialize DMA controllers 0 and 1.		
	Initialize interrupt controllers 0 and 1.		
	Initialize EISA extended registers.		
04	RAM must be periodically refreshed to keep the memory from decaying. This refresh function is working properly.		Get CPU type
05	Keyboard Controller Initialization	The BIOS stack has been built. Next, disabling cache memory.	DMA initialization in progress or failure
CODE	Award	AMI	Phoenix4.0/Tandy3000
06	Reserved	Uncompressing the POST code next.	Initialize system hardware
07	Verifies CMOS is Working Correctly, Detects Bad Battery	Next, initializing the CPU and the CPU data area	Disable shadow and execute code from the ROM.
08	Early chip set initialization	The CMOS checksum calculation is	Initialize chipset with initial POST values
	Memory presence test		
	OEM chip set routines		
	Clear low 64K memory		
	Test first 64K memory		
09	Cyrix CPU initialization		Set IN POST flag
	Cache initialization		
0A	Initialize first 120 interrupt vectors with SPURIOUS-INT-HDLR and initialize INT 00h-1Fh according to	The CMOS checksum calculation is done. Initializing the CMOS	Initialize CPU registers

	INT-TBL.	status register for date and time next.	
0B	Test CMOS RAM Checksum, if Bad, or INS Key Pressed, Load Defaults	The CMOS status register is initialized. Next, performing any required initialization before the keyboard BAT command is issued	Enable CPU cache
0C	Detect Type of Keyboard Controller and Set NUM_LOCK Status	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.	Initialize caches to initial POST values
0D	Detect CPU Clock; Read CMOS location 14h to find out type of video in use. Detect and initialize video adapter.		
CODE	Award	AMI	Phoenix4.0/Tandy3000
0E	Test Video Memory, write sign-on message to screen. Setup shadow RAM ?Enable shadow according to setup.	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test	Initialize I/O component
0F	Test DMA Cont. 0; BIOS Checksum Test. Keyboard Detect and Initialization.	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.	Initialize the local bus IDE
10	Test DMA Controller 1	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command	Initialize Power Management
11	Test DMA Page Registers	Next, checking if <End> or <Ins> keys were pressed during power	Load alternate registers with initial POST values

		on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.	
12	Reserved	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2	Restore CPU control word during warm boot
13	Reserved	The video display has been disabled. Port B has been initialized. Next, initializing the chipset	Initialize PCI Bus Mastering devices
CODE	Award	AMI	Phoenix4.0/Tandy3000
14	Test 8254 Timer 0 Counter 2	The 8254 timer test will begin next.	Initialize keyboard controller
15	Verify 8259 Channel 1 Interrupts by Turning Off and On the Interrupt Lines		
16	Verify 8259 Channel 2 Interrupts by Turning Off and On the Interrupt Lines		BIOS ROM checksum
17	Turn Off Interrupts Then Verify No Interrupt Mask Register is On		Initialize cache before memory Auto size
18	Force an Interrupt and Verify the Interrupt Occurred		8254 timer initialization
19	Test Stuck NMI Bits; Verify NMI Can Be Cleared	The 8254 timer test is over. Starting the memory refresh test next	
1A	Display CPU clock	The memory refresh line is toggling. Checking the 15 second on/off time next	8237 DMA controller initialization
1B	reserved		
1C	Reserved		Reset Programmable Interrupt Controller
1D	Reserved		
1E	Reserved		

1F	If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA tests an clear. EISA mode flag. Test EISA configuration memory Integrity (checksum & communication interface).		
20	Initialize Slot 0 (System Board)		Test DRAM refresh
21	Initialize Slot 1		
22	Initialize Slot 2		Test 8742 Keyboard Controller
CODE	Award	AMI	Phoenix4.0/Tandy3000
23	Initialize Slot 3	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment rewritable and performing any necessary configuration before initializing the interrupt vectors	
24	Initialize Slot 4	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin	Set ES segment register to 4 GB
25	Initialize Slot 5	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.	
26	Initialize Slot 6		
27	Initialize Slot 7	Any initialization before setting video mode will be done next	
28	Initialize Slot 8	Initialization before	Auto size DRAM

		setting the video mode is complete. Configuring the monochrome mode and color mode settings next	
29	Initialize Slot 9		Initialize POST Memory Manager
2A	Initialize Slot 10	Initializing the different bus system, static, and output devices, if present	Clear 512 KB base RAM
CODE	Award	AMI	Phoenix4.0/Tandy3000
2B	Initialize Slot 11	Passing control to the video ROM to perform any required configuration before the video ROM test.	
2C	Initialize Slot 12	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.	RAM failure on address line XXXX*
2D	Initialize Slot 13	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control	
2E	Initialize Slot 14	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next	RAM failure on data bits XXXX* of low byte of memory bus
2F	Initialize Slot 15	The EGA/VGA controller was not found. The display memory read/write test is about to begin	Enable cache before system BIOS shadow
30	Size Base Memory From 256K to	The display memory	

	640K and Extended Memory Above 1MB	read/write test passed. Look for retrace checking next	
31	Test Base Memory From 256K to 640K and Extended Memory Above 1MB	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next	
CODE	Award	AMI	Phoenix4.0/Tandy3000
32	If EISA Mode, Test EISA Memory Found in Slots Initialization	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.	Test CPU bus-clock frequency
33	Reserved		Initialize Phoenix Dispatch manager
34	Reserved	Video display checking is over. Setting the display mode next.	
35	Reserved		
36	Reserved		Warm start and shut down
37	Reserved	The display mode is set. Displaying the power on message next	
38	Reserved	Initializing the bus input, IPL, general devices next, if present	Shadow system BIOS ROM
39	Reserved	Displaying bus initialization error messages.	
3A	Reserved	The new cursor position has been read and saved. Displaying the Hit <DEL> message next	Auto size cache
3B	Reserved	The Hit <DEL> message is displayed. The protected mode memory test is about to start.	
3C	Setup Enabled		Advanced configuration of

			chipset registers
3D	Detect if Mouse is Present, Initialize Mouse, Install Interrupt Vectors		Load alternate registers with CMOS values
3E	Initialize Cache Controller		
3F	Reserved		
40	Display Virus Protest Disable or Enable	Preparing the descriptor tables next	
41	Initialize Floppy Disk Drive Controller and Any Drives		Initialize extended memory for Rom Pilot
CODE	Award	AMI	Phoenix4.0/Tandy3000
42	Initialize Hard Drive Controller and Any Drives	The descriptor tables are prepared. Entering protected mode for the memory test next	Initialize interrupt vectors
43	Detect and Initialize Serial & Parallel Ports and Game Port	Entered protected mode. Enabling interrupts for diagnostics mode next.	
44	Reserved	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.	
45	Detect and Initialize Math Coprocessor	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next	POST device initialization
46	Reserved	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next	Check ROM copyright notice
47	Reserved	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.	Initialize I20 support
48	Reserved	Patterns written in base memory. Determining the amount of memory	Check video configuration against CMOS

		below 1 MB next.	
49	Reserved	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.	Initialize PCI bus and devices
CODE	Award	AMI	Phoenix4.0/Tandy3000
4A	Reserved		Initialize all video adapters in system
4B	Reserved	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.	Quiet Boot start (optional)
4C	Reserved	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.	Shadow video BIOS ROM
4D	Reserved	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next	
4E	Reboot if Manufacturing Mode; If not, Display Messages and Enter Setup	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.	Display BIOS copyright notice
4F	Ask Password Security (Optional)	The memory size display has started. The display is updated during the memory test. Performing the	Initialize Multi Boot

		sequential and random memory test next	
50	Write All CMOS Values Back to RAM and Clear	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.	Display CPU type and speed
CODE	Award	AMI	Phoenix4.0/Tandy3000
51	Enable Parity Checker. Enable NMI, Enable Cache Before Boot	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.	Initialize EISA board
52	Initialize Option ROMs from C8000h to EFFFFh or if FSCAN Enabled to F7FFFh	The memory above 1 MB has been tested and initialized. Saving the memory size information next.	Test keyboard
53	Initialize Time Value in 40h: BIOS Area	The memory size information and the CPU registers are saved. Entering real mode next.	
54		Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next	Set key click if enabled
55			Enable USB devices
57		The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.	
58		The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message next	Test for unexpected interrupts

59		The Hit <DEL> message is cleared. The <WAIT...> message is displayed. Starting the DMA and interrupt controller test next.	Initialize POST display service
5A			Display prompt 'Press F2 to enter SETUP'
CODE	Award	AMI	Phoenix4.0/Tandy3000
5B			Disable CPU cache
5C			Test RAM between 512 and 640 KB
60	Setup virus protection (boot sector protection) functionality according to setup setting.	The DMA page register test passed. Performing the DMA Controller 1 base register test next.	Test extended memory
61	Try to turn on level 2 cache (if L2 cache already turned on in post 3D, this part will be skipped)		
	Set the boot up speed according to setup setting		
	Last chance for chipset initialization		
	Last chance for power management initialization (Green BIOS only)		
	Show the system configuration table		
62	Setup NUM Lock Status According to Setup values	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next	Test extended memory address lines
	Program the NUM lock, typematic rate & typematic speed according to setup setting		
63	If there is any changes in the hardware configuration, update the ESCD information (PnP BIOS only)		
	Clear memory that have been used		
	Boot system via INT 19h		
64			Jump to UserPatch1

65		The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next	
CODE	Award	AMI	Phoenix4.0/Tandy3000
66		Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.	Configure advanced cache registers
67		Completed 8259 interrupt controller initialization	Initialize Multi Processor APIC
68			Enable external and CPU caches
69			Setup System Management Mode (SMM) area
6A			Display external L2 cache size
6B			Load custom defaults (optional)
6C			Display shadow-area message
6E			Display possible high address for UMB recovery
6F			
70			Display error message
71			
72			Check for configuration errors
76			Check for keyboard errors
7C			Set up hardware interrupt vectors
7D			Initialize Intelligent System Monitoring

7E			Initialize coprocessor if present
7F		Extended NMI source enabling is in progress.	
CODE	Award	AMI	Phoenix4.0/Tandy3000
80		The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next	Disable onboard Super I/O ports and IRQs
81		A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next	Late POST device initialization
82		The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.	Detect and install external RS232 ports
83		The command byte was written and global data initialization has completed. Checking for a locked key next	Configure non-MCD IDE controllers
84		Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next	Detect and install external parallel ports
85		The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.	Initialize PC-compatible PnP ISA devices

86		The password was checked. Performing any required programming before WINBIOS Setup next	Re-initialize onboard I/O ports.
CODE	Award	AMI	Phoenix4.0/Tandy3000
87		The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next	Configure Motherboard Configurable Devices (optional)
88		Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next	Initialize BIOS Data Area
89		The programming after WINBIOS Setup has completed. Displaying the power on screen message next	Enable Non-Maskable Interrupts (NMIs)
8A			Initialize Extended BIOS Data Area
8B		The first screen message has been displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next	Test and initialize PS/2 mouse

8C		Programming the WINBIOS Setup options next	Initialize floppy controller
8D		The WINBIOS Setup options are programmed. Resetting the hard disk controller next	
CODE	Award	AMI	Phoenix4.0/Tandy3000
8E		The hard disk controller has been reset. Configuring the floppy drive controller next	
8F			Determine number of ATA drives (optional)
90			Initialize hard-disk controllers
91		The floppy drive controller has been configured. Configuring the hard disk drive controller next.	Initialize local-bus hard-disk controllers
92			Jump to UserPatch2
93			Build MPTABLE for multi-processor boards
95		Initializing bus adaptor ROMs from C8000h through D8000h	Install CD ROM for boot
96		Initializing before passing control to the adaptor ROM at C800	Clear huge ES segment register
97		Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.	Fix up Multi Processor table

98		The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control A	Search for option ROMs. One long, two short beeps on checksum failure
CODE	Award	AMI	Phoenix4.0/Tandy3000
99		Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.	Check for SMART Drive (optional)
9A		Set the timer and printer base addresses. Setting the RS-232 base address next.	Shadow option ROMs
9B		Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.	
9C		Required initialization before the Coprocessor test is over. Initializing the Coprocessor next	Set up Power Management
9D		Coprocessor initialized. Performing any required initialization after the Coprocessor test next.	Initialize security engine (optional)
9E		Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID	Enable hardware interrupts

		command next	
9F			Determine number of ATA and SCSI drives
A0			Set time of day
A1			Check key lock
A2		Displaying any soft error next	
CODE	Award	AMI	Phoenix4.0/Tandy3000
A3		The soft error display has completed. Setting the keyboard typematic rate next.	
A4		The keyboard typematic rate is set. Programming the memory wait states next	Initialize typematic rate
A5		Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next	
A7		NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.	
A8		Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next	Erase F2 prompt
A9		Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next	
AA		Initialization after E000 option ROM control has completed. Displaying the system configuration next	Scan for F2 key stroke

AB		Uncompressing the DMI data and executing DMI POST initialization next	
AC			Enter SETUP
AE			Clear boot flag
CODE	Award	AMI	Phoenix4.0/Tandy3000
B0	If Interrupts Occurs in Protected Mode	The system configuration is displayed.	Check for errors
B1	If Unmasked NMI Occurs, Display Press F1 to Disable NMI, F2 Reboot	Copying any code to specific areas.	Inform RomPilot about the end of POST.
B2			POST done - prepare to boot operating system
B3			
B4			1 One short beep before boot
B5			Terminate QuietBoot (optional
B6			Check password (optional)
B7			Initialize ACPI BIOS
B8			
B9			Prepare Boot
BA			Initialize SMBIOS
BB			Initialize PnP Option ROMs
BC			Clear parity checkers
BD			Display MultiBoot menu
BE	Program chipset registers with power on BIOS defaults		Clear screen (optional)
BF	Program the rest of the chipset's value according to setup (later setup value program)		Check virus and backup reminders
	If auto configuration is enabled, programmed the chipset with predefined values in the MODBINable Auto Table		
C0	Turn off OEM specific cache, shadow		Try to boot with INT 19

	Initialize standard devices with default values: DMA controller (8237); Programmable Interrupt Controller (8259); Programmable Interval Timer (8254); RTC chip.		
C1	OEM Specific-Test to Size On-Board Memory		Initialize POST Error Manager (PEM)
C2			Initialize error logging
CODE	Award	AMI	Phoenix4.0/Tandy3000
C3	Test the first 256K DRAM Expand the compressed codes into temporary DRAM area including the compressed system BIOS & Option ROMs.		Initialize error display function
C4			Initialize system error handler
C5	OEM Specific-Early Shadow Enable for Fast Boot		PnPnd dual CMOS (optional)
C6	External Cache Size Detection		Initialize note dock (optional)
C7			Initialize note dock late
C8			Force check (optional)
C9			Extended checksum (optional)
CA			Redirect Int 15h to enable remote keyboard
CB			Redirect Int 13h to Memory Technologies Devices such as ROM, RAM, PCMCIA, and serial disk
CC			Redirect Int 10h to enable remote serial video
CD			Re-map I/O and memory for PCMCIA
CE			Initialize digitizer and display message
D0		The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.	
D1		Initializing the DMA	

		controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.	
D2			Unknown interrupt
CODE	Award	AMI	Phoenix4.0/Tandy3000
D3		Starting memory sizing next	
D4		Returning to real mode. Executing any OEM patches and setting the stack next.	
D5		Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0	
D6		Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.	
E0		The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test	Initialize the chipset
E1	E1 Setup - Page E1	Initializing the interrupt vector table next	Initialize the bridge
E2	E2 Setup - Page E2	Initializing the DMA and Interrupt controllers next.	Initialize the CPU

E3	E3 Setup - Page E3		Initialize system timer
E4	E4 Setup - Page E4		Initialize system I/O
E5	E5 Setup - Page E5		Check force recovery boot
CODE	Award	AMI	Phoenix4.0/Tandy3000
E6	E6 Setup - Page E6	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.	Checksum BIOS ROM
E7	E7 Setup - Page E7		Go to BIOS
E8	E8 Setup - Page E8		Set Huge Segment
E9	E9 Setup - Page E9		Initialize Multi Processor
EA	EA Setup - Page EA		Initialize OEM special code
EB	EB Setup - Page EB		Initialize PIC and DMA
EC	EC Setup - Page EC		Initialize Memory type
ED	ED Setup - Page ED	Initializing the floppy drive.	Initialize Memory size
EE	EE Setup - Page EE	Looking for a floppy diskette in drive A:. Reading the first sector of the diskette	Shadow Boot Block
EF	EF Setup - Page EF	A read error occurred while reading the floppy drive in drive A:.	System memory test
F0		Next, searching for the AMIBOOT.ROM file in the root directory.	Initialize interrupt vectors
F1		The AMIBOOT.ROM file is not in the root directory	Initialize Run Time Clock
F2		Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file	Initialize video
F3		Next, reading the AMIBOOT.ROM file, cluster by cluster.	Initialize System Management Manager
F4		The AMIBOOT.ROM file is not the correct size	Output one beep
F5		Next, disabling internal cache memory.	Clear Huge Segment
F6			Boot to Mini DOS
F7			Boot to Full DOS

CODE	Award	AMI	Phoenix4.0/Tandy3000
FB		Next, detecting the type of flash ROM.	
FC		Next, erasing the flash ROM.	
FD		Next, programming the flash ROM	
FF	Int 19 Boot Attempt ▼	Flash ROM programming was successful. Next, restarting the system BIOS.	